100% ΔVds TESTED!

100% UIS TESTED!

BV_{DSS}	100		V
I_D@V_{GS}=10V,T_C=25°C	50		A
R_{DSON} ,T_C=25°C	Typ	Max	Unit
@V_{GS}=10V,I_D=20A	12	14	mΩ

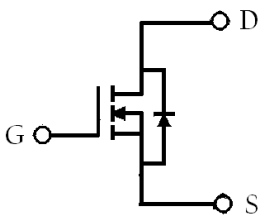
Features

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Description

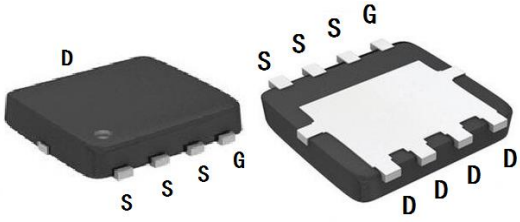
The PSMN040-100MSE-CN is the high cell density trenched N-ch MOSFETs, which provide excellent R_{DSON} and gate charge for most of the synchronous buck converter applications. The PSMN040-100MSE-CN meet the RoHS and Green Product requirement with full function reliability approved.

Equivalent Circuit



Outline

PDFN3.3*3.3



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CT14RN10H	PSMN040-100MSE-CN	PDFN3.3x3.3	-	-	

Table 1. Thermal Characteristic

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction-Case [1]	4.5	℃/W

Table 2. Absolute Maximum Ratings (TA=25℃)

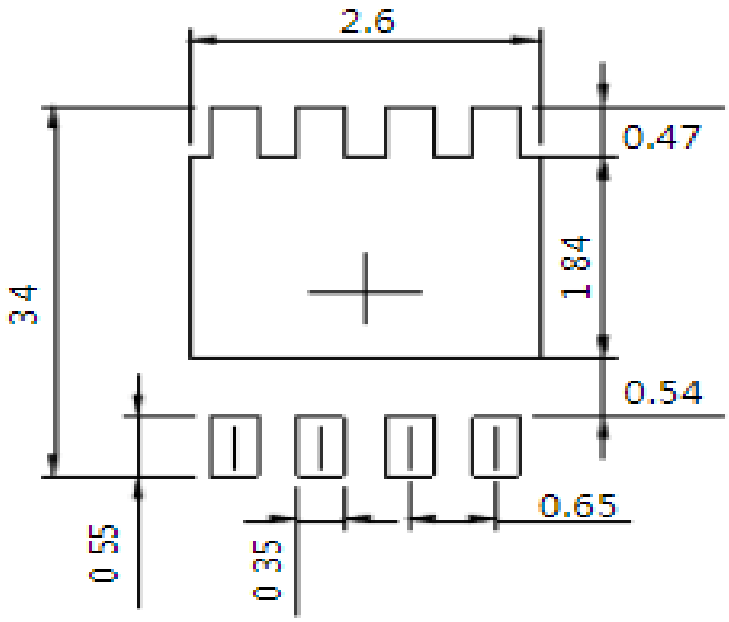
Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (VGS=0V)	100	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
$I_{D\ (DC)}$	Drain Current-Continuous(Tc =25℃) [1]	50	A
	Drain Current-Continuous(Tc =100℃) [1]	32	A
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed [2]	200	
P_D	Maximum Power Dissipation(Tc=25℃) [4]	33	W
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 3. Electrical Characteristics (TA=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	100			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=80V,V_{GS}=0V			1	μA
	Zero Gate Voltage Drain Current(Tc=55℃)	V_{DS}=80V,V_{GS}=0V			5	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance [2]	V_{GS}=10V, I_D=20A		12	14	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=50V,V_{GS}=0V f=1.0MHz		1444		PF
C_{oss}	Output Capacitance			390		PF
C_{rss}	Reverse Transfer Capacitance			15		PF
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V, V_{GS}=10V, I_D=20A, R_G=10Ω		7		nS
t_r	Turn-on Rise Time			26		nS
$t_{d(off)}$	Turn-Off Delay Time			30		nS
t_f	Turn-Off Fall Time			12		nS
Q_g	Total Gate Charge [4.5V]	V_{DS}=50V, V_{GS}=10V, I_D=20A		22		nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			4		nC
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)[1,5]				50	A
V_{SD}	Forward On Voltage [2]	I_{SD}=20A,V_{GS}=0V T_J=25℃			1.2	V
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated				

Notes:
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width≦300us , duty cycle≦2%
3.The EAS data shows Max. rating . The test condition is V_{DD} =50V,V_{GS} =10V,L=0.1mH
4.The power dissipation is limited by 175℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Recommended soldering footprint



unit : mm

Typical Characteristics

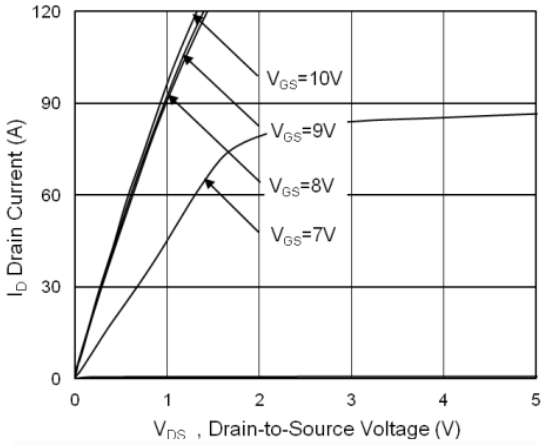


Figure1: Output Characteristics

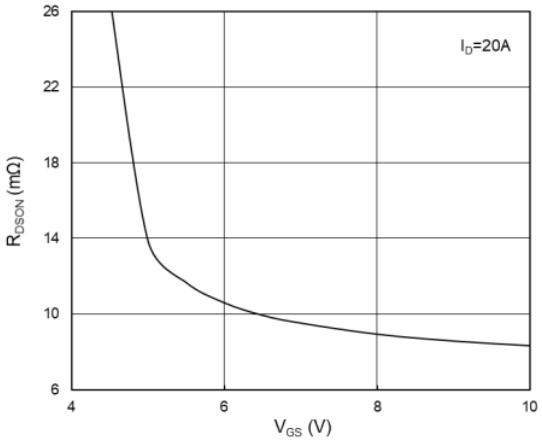


Figure 2: On-Resistance vs. G-S Voltage

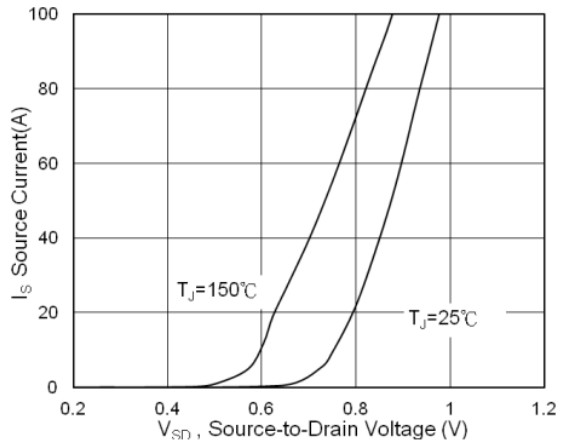


Figure 3: Forward Characteristics of Reverse Diode

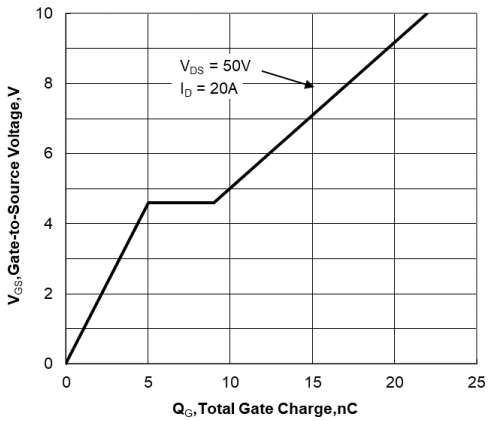


Figure 4: Gate-Charge Characteristics

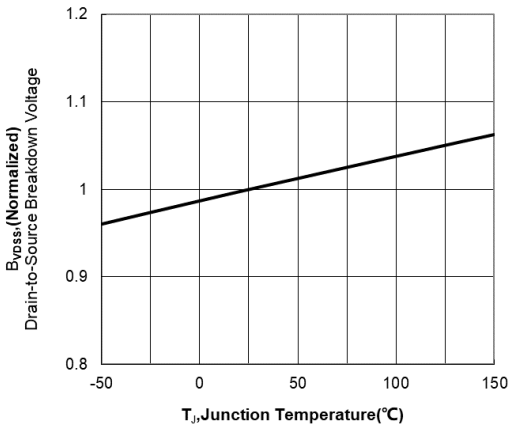


Figure 5: Normalized BVdss vs. Tj

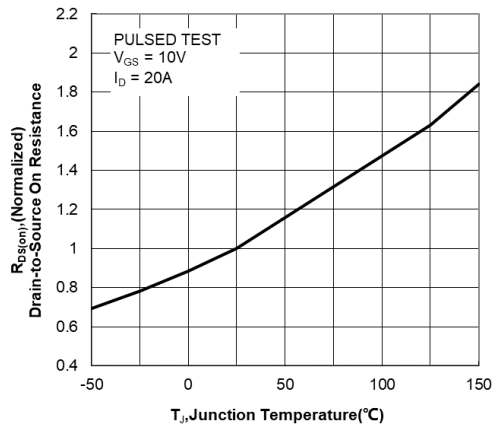


Figure 6: Normalized R_{DSON} vs. T_J

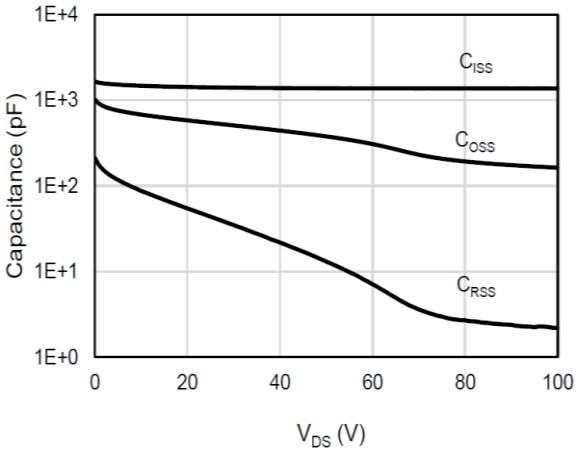


Figure 7: Capacitance

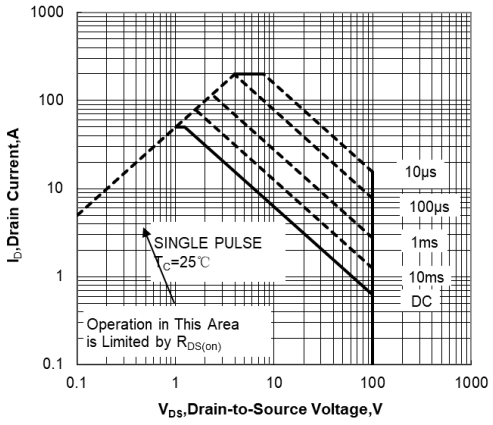


Figure 8: Safe Operating Area

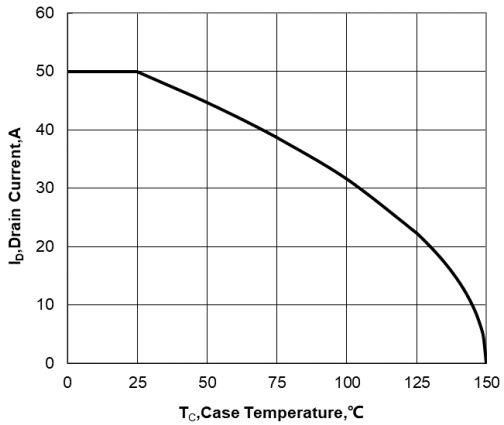


Figure 9: Drain Current

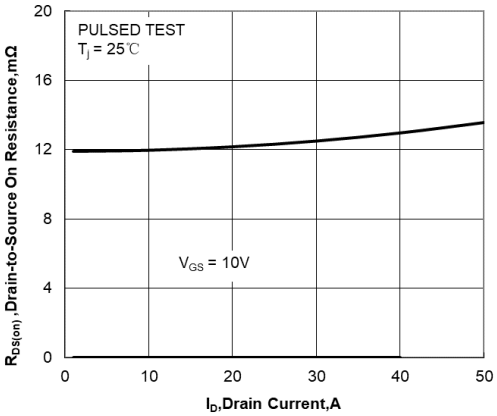


Figure 10: Normalized R_{DSON} vs. Drain Current & Gate Voltage

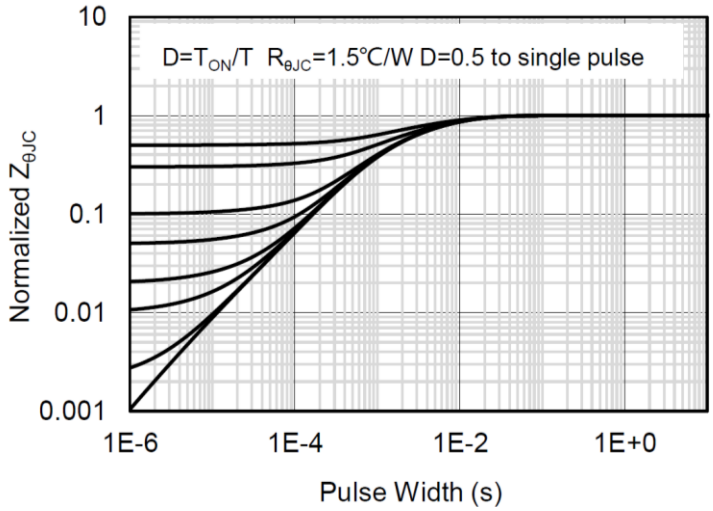
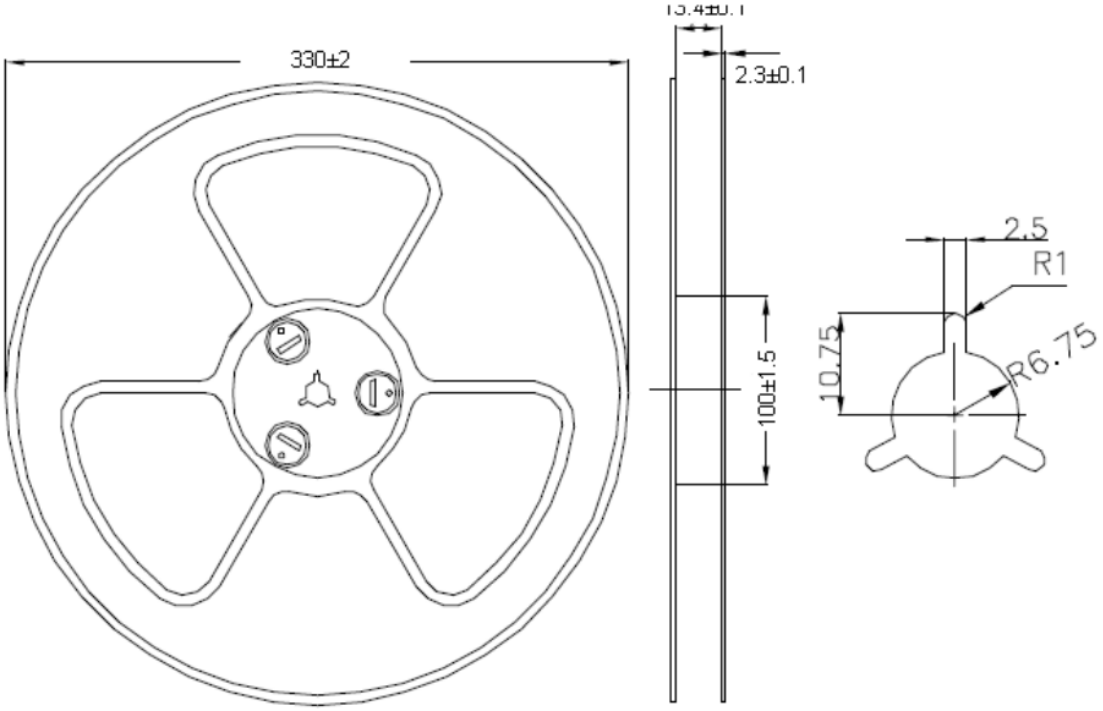
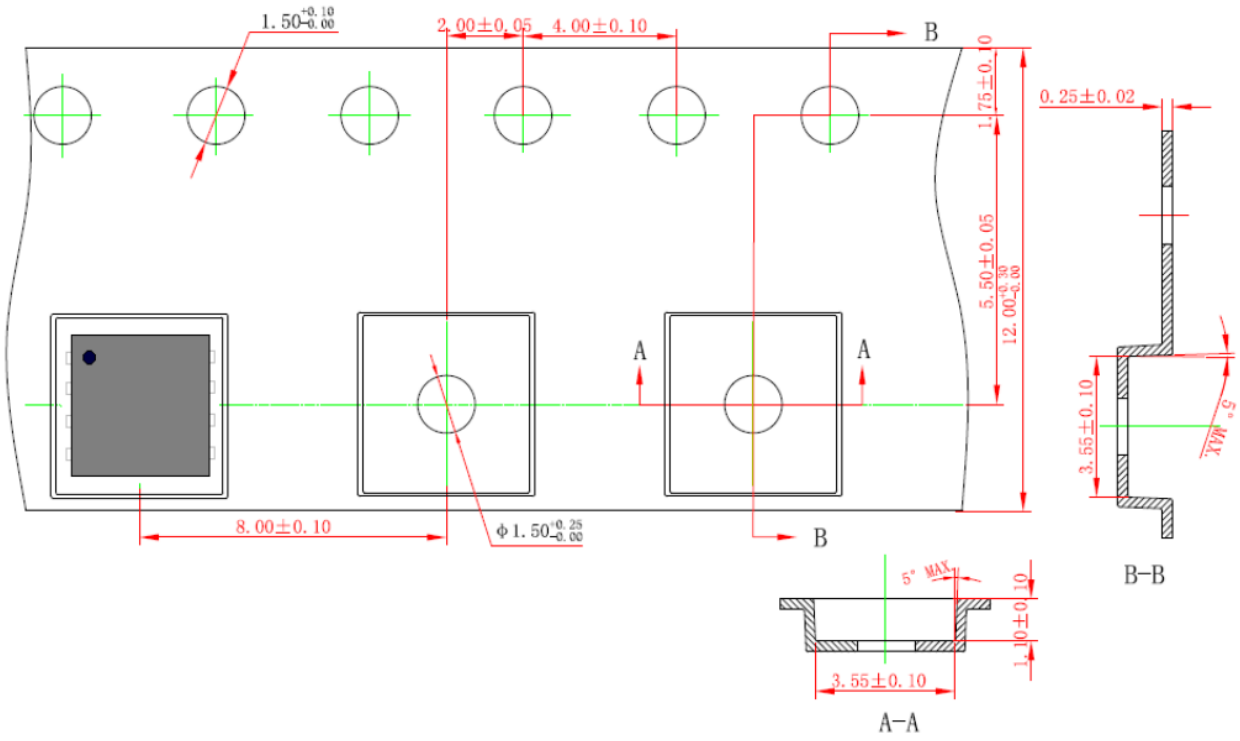


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Reel Dimension



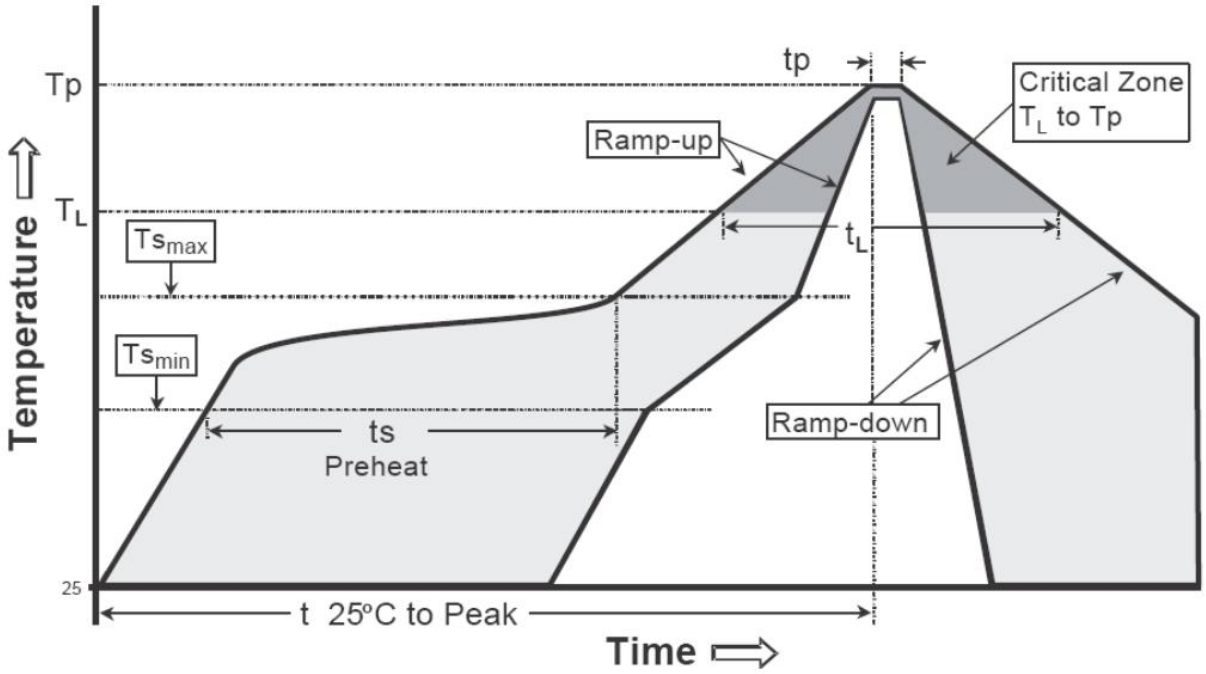
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

Reliability Test item & result

Test Item*	Qualification Test Condition	Test Result						
		EVI		SAM*		F/T		conclusion
		Sample size	Rej / S.S	Sample size	Rej / S.S	Sample size	Rej / S.S	
Before Test	/	220	0/220	10	0/10	220	0/220	PASS
TCT	-65℃~+150℃，168cycles	25	0/25	N/A		25	0/25	PASS
PCT	121℃, 100%RH, 205Kpa, 168hrs	25	0/25			25	0/25	PASS
THT	85℃/85%RH，168hrs	25	0/25			25	0/25	PASS
HTS	150℃, 168hrs	25	0/25			25	0/25	PASS
HTRB	Vd=0.8*BVDSS，恒温 150℃ 168hrs	60	0/60			60	0/60	PASS
HTGB	150℃，100%Vgs 168hrs	60	0/60			60	0/60	PASS

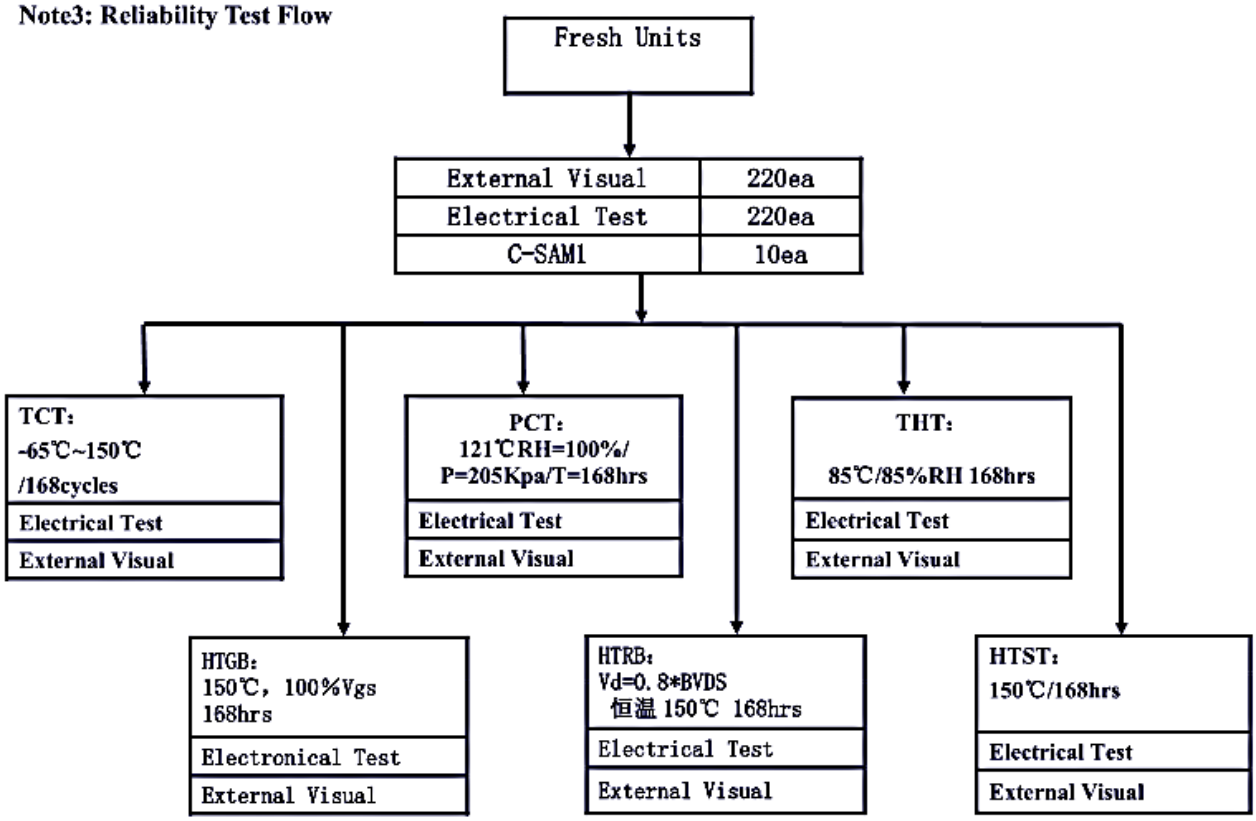
Note1: Test Items*

试验项目 Test Item			参考标准 Reference Standard
TCT	Temperature Cycle Test	温度循环试验	JESD22-A104
PCT	Pressure Cooker Test	高压蒸煮试验	JESD22-A102
THT	Temperature & Humidity Test	恒温恒湿试验	JESD22-A101
HTS	High Temperature Storage Test	高温储存试验	JESD22-A103
HTRB	High Temperature Reverse Bias Test	高温反偏试验	JESD22-A108
HTGB	High Temperature Gate Bias Test	高温栅偏试验	JESD22-A108

Note2: SAM*

SAM data / Test item.	Sample Size	DLMN.（MIN-MAX%）					
		Die		Topside-pad		Topside -lead	
		S.S	%	S.S	%	S.S	%
Before test	10	0	0	0	0	0	0

Note3: Reliability Test Flow



Reliability Evaluation

FIT rate (per billion) ： 237.2(FITS)
MTTF= 481 years
Failure Rate in FIT is calculated according to JEDEC Standard JESD85,Methods for Calculating Failure Rates in Units of FITs, based on accelerated High temperature operating life test results by using an apparent activation energy of 0.7eV.The junction temperature of the device at use is assumed to be 70°C. A constant failure rate is The upper confidence bound of the failure rate is 60%.

Failure Rate = Chi^2 x 10^9 / [2(N)(H)(Af)]=1.833X109 /[2x44x1000x87.8]=237.2
MTTF= 109 / FIT=4215851hrs=481years

Chi^2= Chi Squared Distribution , determine by the number of failure and confidence interval
N= Total Number of units from HTRB and HTGB tests
H= Duration of HTRB/HTGB testing
Af=Acceleration Factor from Test to Use Conditions (Ea=0.7 eV and T Use =70°C)
Acceleration Factor[Af]=EXP [Ea/k(1/Tju-1/Tjs)]

Acceleration Factor ratio list:

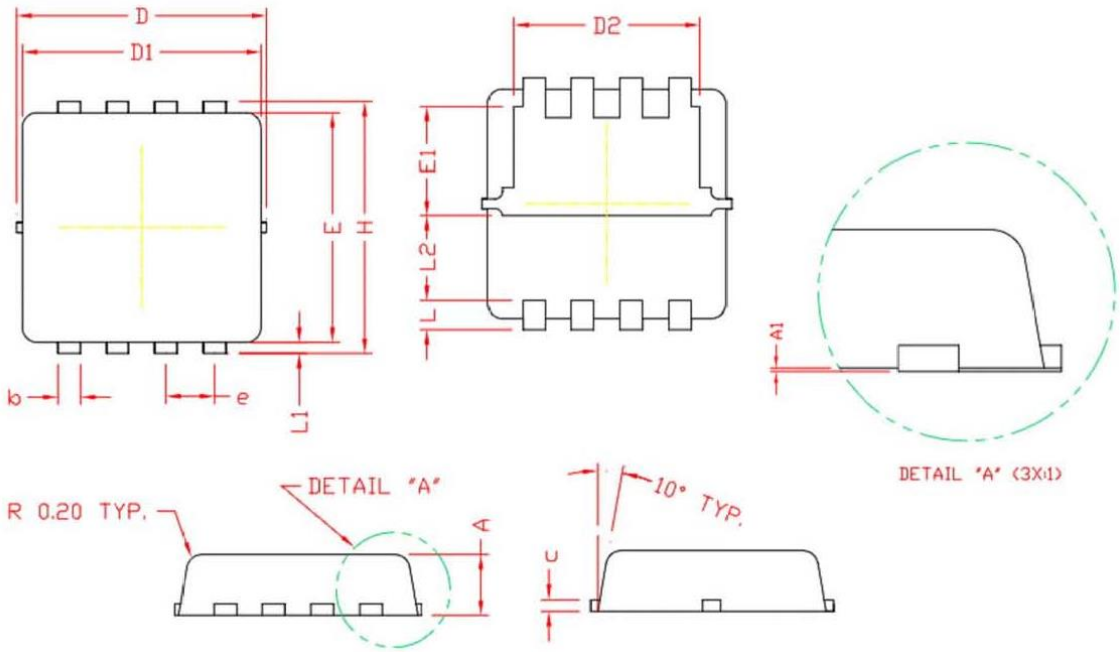
	55°C	70°C	85°C	100°C	115°C	130°C	150°C
Af	259	87.8	32.6	13.1	5.65	2.59	1

Tjs=Stress junction temperature in degree (Kelvin) , K= °C+273
Tju=The use junction in degree (Kelvin) , K= °C+273
K=Boltzmann's constant,8.617164x10^{-5} eV/K

Environmental & Package Stress Test

Test Item	Test Condition	Time Point	Total Sample size	Number of Failures
High Temperature Storage Test(HTST)	Max. Storage Temp=150°C, No bias	168/500/1000 hrs	44 pcs	0
HighTemperature& Humidity Reverse bias (H3TRB)	Temp=85°C, Relative Humidity: 85%R.H. V_{DS}=80% BV_{DSS} Rating	168/500/1000 hrs	22 pcs	0
Temperature Humidity Storage Test (THST)	Temp=85°C, Relative Humidity: 85%R.H. No bias	168/500/1000 hrs	44 pcs	0
Power Cycle Test (PRCL)	ΔTj=90°C,	1K/5K/10K cycles	22 pcs	0
Temperature Cycling Test (TCT)	-65°C,~150°C, ΔT=215°C,	1K cycles	44 pcs	0
Pressure Cooker Test (PCT)	Temp=121°C, Relative Humidity: 100 %R.H. Pressure:2atm	168 hrs	44 pcs	0

PDFN3.3*3.3 Package Information



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.80	0.90
A1	0.00	0.03	0.05
b	0.24	0.30	0.35
c	0.10	0.15	0.20
D	3.25	3.32	3.40
D1	3.05	3.15	3.25
D2	2.40	2.50	2.60
E	3.00	3.10	3.20
E1	1.35	1.45	1.55
e	0.65 BSC.		
H	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.10	0.15	0.20
L2	1.13 REF.		

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